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APPLICATION FOR LETTERS PATENT

for

HIGH DENSITY MODULARITY FOR IC'S

Inventors:
Salman Akram
Jerry M. Brooks

Attorney:
James R. Duzan
Registration No. 28,393
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

HIGH DENSITY MODULARITY FOR IC'S

BACKGROUND OF THE INVENTION

Field of the Invention: This invention relates generally to integrated circuit (IC) or semiconductor devices. More particularly, the invention pertains to integrated circuit configurations which provide high density modules for mounting on circuit boards and other host apparatus.

State of the Art: Integrated circuit semiconductor devices (IC's) are small electronic circuits formed on the surface of a wafer of semiconductor material such as silicon. The IC's are fabricated in plurality as part of a wafer. The wafer is then subdivided into discrete IC chips or dice, and then further tested and assembled for customer use through various well-known individual die testing and packaging techniques, including lead frame packaging, Chip-On-Board (COB) packaging, and flip-chip packaging (FCP). Depending upon the die and wafer sizes, each wafer is divided into a few dice or as many as several hundred or more than one thousand discrete dice, each of which becomes an IC package.

The continuing demand for miniaturization has resulted in the development of integrated circuits on dice of very small size. The corresponding miniaturization of external circuitry has not proceeded at the same rate. Thus, there is a need for devices (including the interconnecting circuitry) of increasingly greater density.

Multi-chip modules have typically followed the convention of earlier, single chip packages, in that the reverse sides of bare dice or chips are mounted on a substrate such as a printed circuit board (PCB), leaving the active surface exposed for wire-bonding to the substrate or ~~leadframe~~ lead frame. Such is exemplified in United States Patent 4,873,615 of Grabbe. Typically, dice are attached to one side only of the substrate, as in United States Patents 4,992,849 and 4,992,850 of Corbett et al.

Where the device encompasses dice on both sides of the substrate, the reverse sides of the dice are conventionally attached to the substrate, as illustrated in United States Patent 5,239,198 of Lin et al.

Stacked groups of packaged devices, often called cubes, have been developed, as exemplified in United States Patent 5,016,138 of Woodman, United States Patent 5,128,831 of Fox, III et al., United States Patent 5,291,061 of Ball, United States Patent 5,420,751 of Burns, United States Patent 5,455,445 of Kurtz et al., United States Patent 5,602,420 of Ogata et al., and United States Patent 5,637,912 of Cockerill et al. In these references, each non-conductive substrate has one or more IC dies attached to one side only, or where dies are attached to both sides of the substrate, not more than one die is so attached on its active surface. In variants where there is no existing substrate between adjacent dice or packages, the packages have peripheral external leads.

In United States Patent 5,291,061 of Ball and United States Patent 5,323,060 of Fogal et al., multiple dice are stacked and wire-bonded to circuitry on a substrate with progressively longer wires.

Dice having ~~areal~~ bond pads, i.e. on the active surface, complicate the construction of multi-chip modules, particularly when wire-bonding is the connection method of choice. As taught in United States Patent 5,012,323 of Farnworth, United States Patents 5,422,435, 5,495,398 and 5,502,289 of Takiar et al., and United States Patent 5,600,183 of Gates, Jr., bonding with wire or other conductor necessitates that the stacked dice be of progressively smaller size.

In United States Patent 4,996,587 of Hinrichsmeyer et al. and United States Patent 5,107,328 of Kinsman, a package is shown with a die within a recess in a carrier. The carrier has shelves which extend over the die, leaving a slot through which the die is wire-bonded to conductive traces on the opposite surface of the shelves. United States Patent 5,677,569 of Choi et al. shows a stacked package in which holes in the substrate permit wire-bonding of die pads to the upper surface of the substrate.

In United States Patent 5,438,224 of Papageorge et al. and United States Patent 5,477,082 of Buckley, III et al., a pair of dice ~~are~~ is shown attached on ~~their~~ its active surfaces to opposite sides of an intermediate layer such as a substrate. In both references, the terminals on the dice are directly coupled to terminals on the same side of the

intermediate member by e.g. solder balls. The opposed dice are shown as being coextensive.

BRIEF SUMMARY OF THE INVENTION

In one aspect, the invention comprises a method for forming a high density multi-chip module (MCM) from a plurality of integrated circuits (IC's) in the form of bare dice with one or more rows of conductive bond pads. The bond pads of each die are preferably formed in a row or rows generally spanning the active surface. The dice are mounted on opposing sides of a substrate in a staggered flip-chip style and wire-bonded through ~~through-slots~~ to conductors on the opposite side of the substrate. Metallization in the form of conductive leads on both surfaces of the substrate is ~~are~~ thus connected by wire bonds to the dice~~,~~ and to an electrical Input/Output (I/O) means such as a ball-grid array (BGA), edge connector, etc. for connection to an external circuit.

In another aspect, the invention comprises the multi-chip module formed by the method.

In one preferred form, an array of solder balls is formed on one surface of the substrate, in the peripheral area surrounding the die or dice mounted on that surface. Alternatively, a pin-grid array may be used. The multi-chip module may be readily attached by surface mounting on a circuit board, for example.

In another preferred form, an edge connector such as a socket connector as well-known in the art may be used.

The bonded wires within the through-slots in the substrate are preferably surrounded with a "glob-top" sealant material following testing. Thus, the wire connections are sealed by glob-top on one side of the substrate~~,~~ and by the die bonding material on the opposite side of the substrate. A minimum amount of glob-top material is required.

The module construction permits testing of each die after wire-bonding~~,~~ and easy removal and replacement of a defective die, if necessary, without removal of any encapsulant material. The construction is such that the bonded conductive wires are,

prior to glob top application, protected from physical damage by their location within through-slots in the substrate, and between or adjacent opposing dies. The opportunity for damage during die testing or die replacement prior to wire encapsulation is greatly reduced.

The module of the invention has a high density, inasmuch as it is formed as an array of bare dice rather than encapsulated packages of greater size. Dice are mounted on both sides of a substrate to form the module, and coplanar dies may be closely spaced, leaving room enough for forming the wire-bonds within the through-slots.

The method of the invention may be employed to surface mount bare dice on e.g. a printed circuit board of an electronic component.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated in the following exemplary figures, wherein the drawings are not necessarily to scale.

FIG. 1 is a perspective upper view of a high density IC module of the invention;

FIG. 2 is a perspective lower view of a high density IC module of the invention;

FIG. 3 is a top view of a high density IC module of the invention, in an intermediate stage of fabrication;

FIG. 4 is a bottom view of a high density IC module of the invention, in an intermediate stage of fabrication;

FIG. 5 is a cross-sectional edge view of a high density IC module of the invention, as taken along line 5-5 of FIG. 1;

FIG. 6 is a cross-sectional edge view of a high density IC module of the invention, as taken along line 6-6 of FIG. 5;

FIG. 7 is a partial cross-sectional view of another embodiment of a high density IC module of the invention;

FIG. 8 is a partial cross-sectional view of another embodiment of a high density IC module of the invention;

FIG. 9 is a top view of a high density IC module of the invention, in an intermediate stage of fabrication;

FIG. 10 is a bottom view of a high density IC module of the invention, in an intermediate stage of fabrication; ~~and~~

FIG. 11 is a perspective top view of another embodiment of a high density IC module of the invention~~.~~;

DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

An exemplary embodiment of the invention is illustrated in drawing FIGS. 1 through 8 and is shown as a high density module 10 having two IC dies 12A, 12B mounted on a first side 16 of a substrate 20. One IC die 14A is shown on the opposite (second) side 18 of the substrate, in a staggered position relative to dies 12A, 12B. While the figures show a total of three dies 12A, 12B, 14A a1 in the module, any number may be mounted to substrate 20 to form a dense IC module for use as a memory device, for example. ~~In a spacially balanced module, the numbers of dice on the first and second sides 16, 18 will differ by one.~~

The dice 12, 14 are attached to the substrate 20 by an adhesive layer 38, which may be any non-conductive adhesive or adhesive tape as known in the art.

~~Each of the IC dies 12A, 12B and 14A is a bare (unpackaged) die with one or more adjacent rows of bond pads 22 on an active~~ ~~side~~ surface thereof ~~24. In drawing FIGS. 1 and 2, the bond pads 22 of dies on the opposite side are not visible, being covered by a glob-top 40. In drawing FIGS. 5 to 8, two rows of bond pads 22 are shown spanning the minor dimension 26 of the dies (~~~~See~~ see ~~FIG. 1). Alternatively, the bond pads 22 may be configured in a row or rows anywhere on the active surface 24, but preferably along a centerline 42 of a major dimension 28 or minor dimension 26, or even at an oblique angle with the major dimension 28. Preferably, the dice 12, 14 should be aligned so that the rows of bond pads 22 are in a parallel, spaced-apart relationship.~~

The substrate 20 is shown with elongate through-slots 30A and 30B, each through-slot passing through the substrate between the first side 16 and the second side

18. The through-slots 30A, 30B are configured to provide access from the opposite side 18 of the substrate 20 for wire-bonding the bond pads 22 to connection sites 32 of a conductor pattern 34 on the substrate. The dice 12A and 12B are spaced a distance 36 apart, leaving room for the through-slot 30C therebetween.

As shown in drawing FIGS. 2 and 4 through 8, die 14A is mounted on the opposite side 18 of the substrate 20 between through-slots 30A and 30B. Like dice 12A and 12B, die 14A has its active surface 24 bonded to the substrate 20. Through-slot 30C encompasses the bond pads 22 of die 14A and is configured to provide access to the bond pads from the first side 16 of the substrate 20, i.e. from the side opposite the side to which the die 14A is attached.

Conductor patterns 34A, 34B are incorporated on each side 16, 18, respectively, of the substrate 20, having connection sites 32 adjacent each through-slot 30 for wire-bonding to bond pads 22 with conductive wires 44. The conductor patterns 34A, 34B and connection sites 32 are not shown in drawing FIGS. 1 through 4 for the sake of clarity, but are depicted in drawing FIGS. 5 through 8.

An exemplary conductor pattern 34A is shown on first substrate side 16 in drawing FIG. 9. The conductor pattern 34A has connection sites 32A for wire-bonding to die 14A (not shown in FIGS. 9 and 10) through through-slot 30C. In the example shown, the conductors 35A of conductor pattern 34A are also connected to solder balls 50 on side 18 (~~See~~ see FIG. 2) which comprise input/output connections for connecting the dice 12, 14 to external circuitry. The solder balls 50 comprise a ball-grid-array in a peripheral area 46 surrounding the die or dice. The balls are configured to be surface mounted to conductive traces on a larger substrate such as a circuit board, not shown. The input/output connections may also comprise a pin-grid-array (PGA), such an array being well known in the art.

The conductor pattern 34A on side 16 of the substrate 20 is interconnected with the solder balls ~~40~~ 50 or with conductor pattern 34B on side 18 by conductive vias 48 passing through the substrate.

The conductor pattern 34B has connection sites 32B for wire-bonding to dice 12A and 12B (not shown in FIGS. 9 and 10)~~)~~ through through-slots 30A and 30B, respectively. In the example shown, the conductors 35B of conductor pattern 34B have outer ends 52B which are connected to solder balls 50 on the same side 18 (~~See~~ see FIG. 2).

As shown in drawing FIGS. 1 through 10, the module 10 has a separate solder ball 50 conductively connected to each bond pad 22 of the three dice 12A, 12B, 14A. Where the dice are to have common conductors, the number of solder balls 50 or other input/output connection lines will be much decreased.

A socket type connector 54 may be used instead of the ball-grid-array of balls 50, or pin-grid-array. As shown in drawing FIG. 11, a socket type connector 54 may be provided which permits vertical placement of the module on a circuit board, or cable connection. The conductor patterns 34A, 34B will vary from those of drawing FIGS. 9 and 10 in that the conductors 35A and 35B will extend to the socket type connector 54 rather than to an array of solder balls 50. Methods for making such patterns and connections are well known in the art.

Turning now specifically to drawing FIGS. 5 through 8, several variations in the through-slot configuration are illustrated.

A simple through-slot configuration in drawing FIGS. 5 and 6 has flat walls 56. The walls 56 are shown as parallel, but in an alternative arrangement, they may be beveled relative to each other. The through-slots 30A, 30B and 30C are shown with wires 44 bonded to bond pads 22 and connection sites 32A, 32B on substrate sides 16 and 18, respectively. The slot width 62 is such that it exposes the bond pads 22 and permits entrance of a wire bonding machine head for bonding the conductive wires 44. The slot length 60 exceeds the length of the row of bond pads 22, providing space for performing the wire-bonding.

Drawing FIGS. 7 and 8 correspond generally to drawing FIG. 5, but show different through-slot configurations, and do not show the glob-top 40. As depicted in drawing FIG. 7, through-slot 30C is formed with outwardly extending stepped surfaces 58 in opposed walls 56. These stepped surfaces 58 face the opposite side 16 of the substrate

20, and connection sites 32A on the stepped surfaces 58 are wire-bonded to bond pads 22 on die 14A with wires 44. In this configuration, stepped surfaces 58 are only slightly recessed from the substrate side 16.

In drawing FIG. 8, each through-slot step 58 is positioned much deeper in the substrate 20, shortening the length of the wires 44.

In drawing FIGS. 7 and 8, the wires 44 are effectively buried within the substrate 20, making them less prone to physical damage during handling of the module.

The method of making the module 10 of the invention comprises the following steps:

A plurality of integrated circuit dice 12, 14 is ~~are~~ procured or fabricated. The integrated circuit dice 12, 14 are formed with an active surface 24 with one or more rows of conductive bond pads 22 thereon.

A planar substrate 20 having first side 16 and opposing side 18 is formed, and at least three through-slots 30 are formed in the substrate wherein each through-slot has a length 60 and width 62 sufficient to expose the rows of bond pads 22 of a die 12 or 14 bonded to the substrate to overlie the through-slot. The through-slot may be of uniform width 62, or may include a stepped surface(s) 58.

Conductor ~~Conductive~~ patterns 34A, 34B are formed on sides 16,18, respectively, of the substrate 20, such as by a lithographic metallization process or by other methods known in the art. The Conductor ~~conductive~~ patterns 34A, 34B include conductors 35 having one end configured as a wire-Connection ~~connecting~~ site 32 adjacent a through-slot 30, and the other end is configured for attachment to an input/output connection. Where the through-slot 30 is stepped, the wire-Connection ~~connecting~~ sites 32 are positioned on the stepped surfaces 58.

The formation of the through-slots 30 and the conductive patterns 34A, 34B may be in any order.

An input/output connection means is added to the module 10 and may comprise an array of solder balls 50 or pins, or may be a socket type edge connector 54.

Dice 12, 14 are then mounted on both sides 16, 18 of the substrate 20 with an adhesive layer 38. Each die is mounted so that all of its bond pads 22 to be connected are

positioned within a through-slot 30 and are thus exposed on the opposite side of the substrate 20 between two other dice, for wire-bonding.

Bond pads 22 of each die 12, 14 are wire-bonded by conductive wires 44 to the connecting sites 32 of the conductor patterns 34A, 34B.

Typically, each die 12, 14 and/or all dice collectively are tested for operability before the through-slots 30 are filled with glob-top 40 to encapsulate and seal the wires 44 therein and spaces between adjacent dice 12, 14.

Optionally, the module, including the otherwise exposed die surfaces and substrate, may be encapsulated with a polymeric material.

The module 10 as described has a high density. The effective density increases as the number of dice 12, 14 is increased. Both sides of the substrate 20 are utilized, and the modules 10 so formed may be surface bonded to both sides of a printed circuit board (PCB), for example. Furthermore, the method may be used as chip-on-board (COB) technology for attaching a plurality of bare dice 12, 14 to a mother board without prior encapsulation.

The wire protection provided by the through-slots 30 and dice 12, 14 enables the module 10 to be electrically tested prior to glob-top encapsulation, without endangering the wires 44. This also enables easy and rapid removal and replacement of any defective die.

The method requires minimal glob-topping.

Additional advantages and modifications will readily be recognized by those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and representative devices, shown and described herein, but includes various modifications which may be made without departing from the spirit or scope of the general inventive concept and embodiments as defined by the appended claims and their equivalents.